A Low-Loss Ka-Band Distributed MEMS 2-Bit Phase Shifter Using Metal-Air-Metal Capacitors

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Abstract — **A two-bit wideband distributed CPW phase shifter has been developed on a 500 μm quartz substrate for Ka-band operation. The design utilizes MEMS switches in a DMTL (Distributed MEMS Transmission Line) periodically loaded by MEMS switches and high Q ($>$ 250 at 30 GHz) metal-air-metal capacitors. The MEMS switches are actuated by a low 20 volt P-P AC bias voltage via a high-resistance bias line. Estimated spring constant and switching time of the MEMS switch is 30 N/m and $\sim$ 9 μs, respectively. The two-bit design results in a reflection coefficient better than -11.5 dB, an average insertion loss of -1.5 dB, and phase shifts of 89°, 180°, and 270° at 37.7 GHz. This is currently the lowest loss distributed phase shifter at Ka-band frequencies.**

I. INTRODUCTION

Distributed phase shifters operate on a principle of dispersion. By increasing the distributed capacitance on the t-line (transmission line), the phase velocity decreases, thus providing a differential phase shift. There have been many recent demonstrations of this type of phase shifter [1]-[2] at 10 GHz (X-band) using CPW and microstrip lines. As in the previous designs, MEMS switches are used to change loading capacitance on a high-impedance transmission line ($>$ 50 Ω) such that the return loss is within an acceptable range for the two phase states (with the MEMS switches in the up and down-state positions). Generally, the loaded impedances are 60 Ω and 41.7 Ω for a -15 dB of return loss per bit. The ultimate goal of these designs is to provide the maximum amount of phase shift at the minimum amount of insertion loss with a return loss of less than -10 dB.

The design contained here is the first demonstration of a DMTL phase shifter at 30-40 GHz (Ka-band) using MEMS switches. The design reflects what has been learned from previous attempts in terms of minimizing insertion loss, which will be discussed in more detail in Section II. Also, compared to previous designs, high-resistivity bias lines have been introduced for easier and lower voltage electrostatic actuation. The bias lines and their effect is discussed in Section IV.

Other work in this area include the first demonstration of a CPW distributed "analog" phase shifter at 75-110 GHz using MEMS varactors [3]. A demonstration of a 16 GHz microstrip "digital" phase shifter, in which the MEMS switches have only two states, up and down, is presented in [2]. An excellent, yet narrowband and having 13° of maximum phase shift error, MEMS switched line, Ka-band (f_o = 34 GHz) phase shifter [4] has an average insertion loss of 1.7 dB and 2.3 dB for 3 and 4-bit designs, respectively. Also, to the authors' knowledge, Kim will present a "digital" distributed phase shifter at 60 GHz using similar techniques to those presented in this paper [5].

II. DESIGN OF THE DMTL PHASE SHIFTER

A photograph of the phase shifter unit cell is in Figure 1 and shows a MEMS switch suspended over the 150 μm wide center conductor of a CPW line. The CPW gap is 150 μm and the DMTL is fabricated on a quartz ($\epsilon_r = 3.6$) substrate. The MEMS switch is anchored within the CPW gap and is connected to a thin-film bias-line resistor. The MEMS switch is also connected to a short t-line, which ultimately forms the bottom metal of the MAM (Metal-Air-Metal capacitor). The MAM capacitor is plated on three sides thus providing a very high Q, very rigid, stable capacitor. The sacrificial layer underneath the MAM capacitor is PMMA.

The impedance of the unloaded line without these MAM cuts in the ground plane is approximately 98 Ω. However, fringing capacitance due to the ground-plane cuts lowers the t-line impedance to $\sim$ 72 Ω. The additional fringing is accounted in the size of the MAM capacitors. Test structures show the combined Q of the fringing and MAM capacitance to be $\sim$ 300.

With the MEMS switch in the up-state position, the loading capacitance seen by the high-impedance line is the series combination of the MEMS switch (C_b) and the total capacitance of the MAM and fringing capacitance (C_s), and is $C_l = C_s C_b/(C_s + C_b)$. When a bias voltage is applied between the MEMS switch and the high-impedance line using a thin-film resistor, the MEMS switch capacitance increases by a large factor and the loading to the line therefore becomes dominated by the MAM capacitor and the fringing capacitance.

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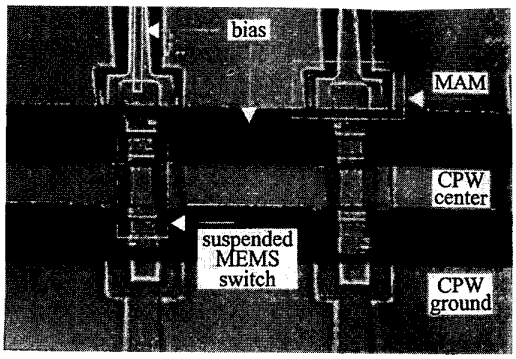

Fig. 1. Photograph of the DMTL phase shifter showing two unit cells after electroplating, thus forming the MAM capacitor.

The phase shift of the slow-wave structure is derived to be [1]:

$$\Delta\phi = \frac{\omega Z_o \sqrt{\epsilon_{r,eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right) \quad \text{rad/m}$$

where Z_{lu} and Z_{ld} are the distributed DMTL loaded impedances, Z_o is the characteristic impedance of the high impedance CPW line, and $c/\sqrt{\epsilon_{r,eff}}$ is the high impedance line guided velocity. The design starts with closed-form expressions for phase shift, MEMS separation, and loading capacitors, but true modeling is best achieved by the software package Sonnet [6], a method of moments simulator which is found to produce extremely accurate simulations of these distributed circuits.

III. TWO-BIT PHASE SHIFTER: DESIGN AND MEASUREMENTS

A photograph of the entire two-bit phase shifter is shown in Figure 2. It consists of two sections, and each section is connected to its own bias line. The first section has 7 switches and is designed to have $\Delta\phi = 90°$ at 30 GHz. The second section has 14 switches and is designed to have $\Delta\phi = 180°$ at 30 GHz. Differential phase shifts of 90°, 180°, and 270° result from applying a 20 volt P-P AC bias voltage to the individual sections. Each section is designed for a maximum return loss of -15 dB, thus providing a cascaded performance of better than -10 dB over all four states.

The design above was developed for a MEMS switch and a MAM capacitor with a height of 1.5 μm. The fabrication procedure used for the MEMS switch was changed in hopes of producing a lower stress bridge and this was accomplished by removing certain metals from the switch, and using a sacrificial layer of 2.1 μm. The resulting spring

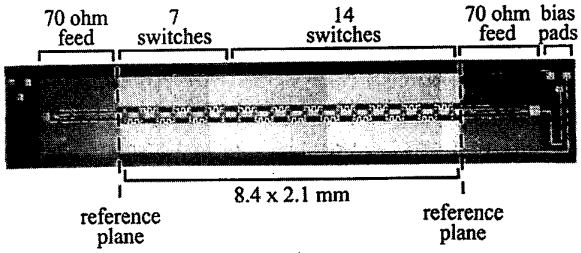

Fig. 2. Photograph of the entire 2-bit, Ka-band, 21 switch, DMTL phase shifter.

constant is 30 N/m with pull-in voltage V_p = 13-14 V and the switching time of the MEMS switch is calculated [7] to be 9 μs for a switching voltage of V_s = 20 V. However, there were new challenges to the fabrication procedure: the MEMS switch lowered to 1.2 μm while the MAM capacitor remained at 2.1 μm. The exact reason for this movement is under investigation, but the movement is consistent over all 21 bridges, and was measured by a light-interferometer microscope. As a result, the loaded impedances are shifted from the intended 60 Ω and 42 Ω to 62 Ω and 48 Ω.

The measured results therefore do not operate at 30 GHz, but the distributed design is so wideband, that proper operation was achieved around 38 GHz. Figure 3 shows the measured two-bit performance of the DMTL MEMS phase shifter, with differential phase shifts of 89°, 180°, and 270° at 37.7 GHz. All states have a return loss of better than -11.5 dB, with a worst-case insertion loss of -2.1 dB. The average insertion loss is only -1.5 dB.

Simulation using the new measured suspended heights agree quite well with measurements, as seen in Figure 4. Also modeled by the simulation is the loss due to the thin film Si-Cr resistor, whose effect is discussed in the next section.

IV. BIAS LINES AND LOSS

The biasing of each bit is achieved using a single high-resistance line which is attached to one of the bridges in the bit, and then moving the bias from bridge to bridge using a meandering thin-film high-resistance line (see Figure 2). The meandering bias lines still have a significant effect on the overall insertion loss performance of the phase shifter. The bias lines are sputtered from a silicon-chrome target and are defined by wet etching (BHF). The resulting lines are 20 μm wide, 1,500 $\AA$ thick, and approximately 610 μm long. The conductivity of the material is 2,150 S/m, thus resulting in a resistance of 23.7 KΩ. Sonnet simulations demonstrate the phase shifter would have a maximum insertion loss of -1.1 dB at 37.7 GHz if no bias lines were

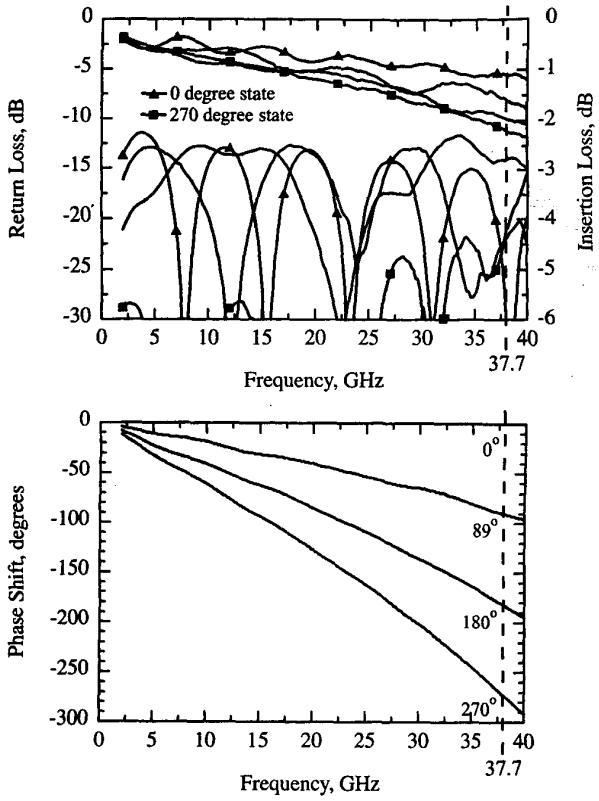

Fig. 3. Measurement of the Ka-band, 2-bit, DMTL phase shifter. Return loss is better than -11.5 dB, and the average insertion loss is -1.5 dB at 37.7 GHz where 89°, 180°, and 270° of phase shift is achieved.

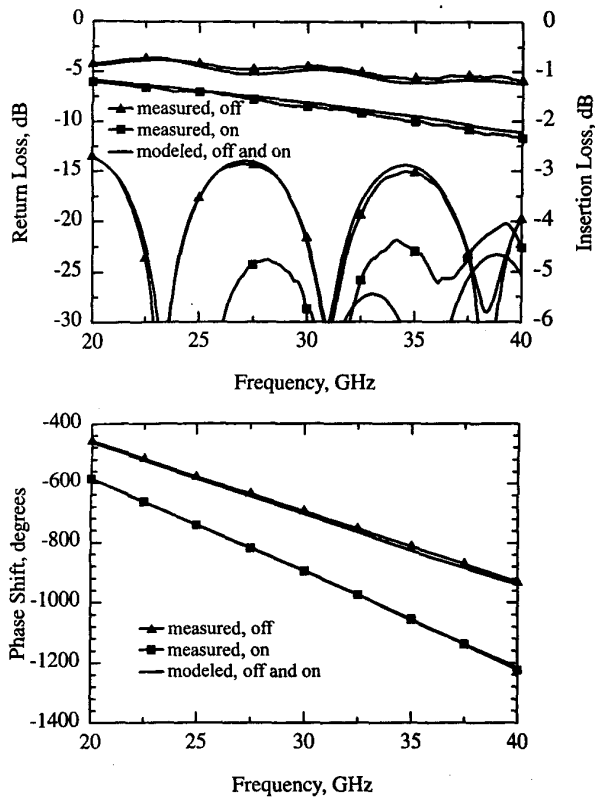

Fig. 4. Measurement (with symbols) and simulation of the 21 switch DMTL phase shifter with all switches either on or off.

present.

Effectively, the MAM capacitors "see" two of these resistances in parallel because there are two bias lines attached to each switch (Fig. 1). Additionally, where the bias lines feed underneath the CPW ground and contact the first switch in a phase bit, the capacitor Q is further reduced by another resistance in parallel with the two mentioned above. This small resistor is modeled as a 30 μm long section of resistive line because the Si-Cr line strongly couples to the ground plane by means of the air bridge over it. The effective resistance of this short section is 1.16 KΩ.

The design has a static capacitance is $C_s = 66$ fF and using a Q of 300 at 37.7 GHz, $R_p = 19.2$ KΩ. By adding the resistance (R_b) of two parallel bias lines in parallel with R_p, the Q is effectively reduced from 300 to 110. The Q at the 2 points (out of 21) where bias lines are fed inside the CPW is reduced to around 15. The reduction in the capacitor Q increases the maximum measured loss from an ideal value of -1.1 dB to the measured value of -2.1 dB at 37.7 GHz.

V. CONCLUSIONS

This paper presented a very low-loss Ka-band distributed phase shifter. The bridge height was incorrect, and this moved the design frequency from 30 GHz to 37.7 GHz. Still, the concept of using a very high Q MAM capacitor in series with a low loss MEMS switch is proven in this work. The design can be easily scaled to 60 GHz or 77 GHz for communications and automotive applications.

ACKNOWLEDGEMENT

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